IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Accompanying Continuation Application under 37 CFR 1.53(b):

Prior Application:	Y. OKAMOTO et al USSN 09/567,158 Filed: May 9, 2000
Group Art Unit:	1756
Examiner:	N. BARRECA
For:	PROCESS FOR FABRICATING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, AND EXPOSING SYSTEM AND MASK INSPECTING METHOD TO BE USED IN THE PROCESS

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

August 7, 2001

Sir:

Prior to examination, please amend the above application as follows.

IN THE CLAIMS

Please cancel claim 1 and add new claim 39 as set forth below.

39. (New) A method of making a semiconductor device, comprising the steps of:

(i) irradiating a mask, where an enlarged circuit pattern is formed, with an exposure light flux, being at least partially coherent in the ultraviolet domain; and

(ii) reducing and projecting the exposure light flux passing through the mask, by an optical reducing projection exposure system, so that a desired reduced circuit pattern corresponding to the enlarged circuit pattern can be focused onto a photosensitive resist film overlying a major surface of a wafer, whereby the reduced circuit pattern corresponding to the enlarged circuit pattern is transferred onto the wafer, said mask comprising:

(a) a transparent mask substrate having a first and a second major surfaces;

(b) a first opening region having an inner corner portion and an outer corner portion in a light shielding region over the first major surface of the mask substrate, which inner corner portion borders on a vertex portion of the light shielding region, which outer corner portion borders on a vertex portion of the first opening region, and which first opening region corresponds to the reduced circuit pattern to be transferred onto the wafer;

(c) an auxiliary light shielding region having a size smaller than that of the first opening region, in the first opening region over the first

major surface of the mask substrate, which auxiliary light shielding region is disposed at the vertex portion of the light shielding region, and has such a size that the auxiliary light shielding region reduces deformation of the transferred pattern onto the wafer corresponding to the first opening region by reducing the light intensity on the wafer at the inner corner portion of the first opening region without affecting the whole shape of the transferred pattern onto the wafer corresponding to the first opening region; and

(d) an auxiliary opening region having a size smaller than that of the first opening region, in the light shielding region over the first major surface of the mask substrate, which auxiliary opening region is disposed at the vertex portion of the first opening region, and has such a size that the auxiliary opening region reduces deformation of the transferred pattern onto the wafer corresponding to the first opening region by enhancing the light intensity on the wafer at the outer corner portion of the first opening region without affecting the whole shape of the transferred pattern onto the

wafer corresponding to the first opening region, and the phase of which auxiliary opening region is the same as that of the first opening region.

REMARKS

The Applicants request entry of the foregoing new claim.

Respectfully submitted,

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